Controlling Method and Device for Data Transmission

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The invention relates to the field of data buffer, and more particularly to a controlling method and device for data transmission in the dual buffer architecture.

2. DESCRIPTION OF THE RELATED ART

To satisfy the higher demand of the quality of the audio and video image, the corresponding multimedia standards have been built up. Since the multimedia data usually require more space to storage and bandwidth to transmit, the corresponding buffer which set up in a player as a data transmission channel is in great demand than before. However, due to the conventional transmission channel devices typically lack of planning such that the switch and intercommunication was impeded and then lower the overall performance.

With regard to the above-mentioned, figure 1A is a schematic diagram illustrating the method and device of a buffer as a data transmission channel based on the related art including a data transmission channel 100 as a data buffer that constructed between a host and a peripheral such as a CD-R drive or a CD-RW drive, or constructed in a DVD Player or DVD Recorder, and a system bus 110 coupling to the host. When the system command is "Host Read", the data sequentially sent to and cached in the data transmission channel 100 before decoding and consequent transmission procedures. However, while the bus adjusting the direction

according consequent system command, the data cached in the data transmission channel 100 may be discarded (i.e. "Flush") so that the data transmission channel 100 which as a common area for temporary storage employed by the data of the successive commands, and the corresponding index modifying its value frequently and terminated all the data processing procedures of the formal command when the last one begin to perform. Consequently, when the incessant switch between random two commands occur frequently, the data transmission channel 100 will result in the shortcomings that consuming the transmission time, transmission not smooth, and lower the performance while waiting the mechanical components to access data, flushing the content of the buffer, re-seeking the raw data, modifying the content of the corresponding indices, etc.

Figure 2 representing a flowchart of the method for the data transmission channel based on the prior art including steps 210 to 250. At first, Step 210 indicates that the first command data processing procedures based on the first command to transmit the data between the data transmission channel 100 and the bus 110. It's noted that when the first command is "Host Read", the data of the data transmission channel 100 flows into the bus 110, and the corresponding consequent data processing procedures including of caching data in the data transmission channel 100, decoding (in the channel CODEC), and sending the decoded data away form the data transmission channel 100. On the other hand, when the first command is "Host Write", the data of the bus 110 flows into the data transmission channel 100, and the corresponding consequent data processing procedures including caching data in the data transmission channel 100, encoding (in the channel CODEC), sending the encoded data away form the

data transmission channel 100 and performing related recording procedures. Second, the bus 110 adjusting the transmitting direction in step 220 through comparing the second command to the first one, and taking step 230 for retrieving and caching the data of the second command in the data transmission channel 100 that the location of the cached data will follows the one of the first command since these two commands are the same, otherwise taking step 240 to discard the data of the first command that cached in the data transmission channel 100, and performing the related procedures in step 250. It's noted that the parts of processing procedures of the first command will terminate when the data processing procedures of the second command began to perform, or it will result in the problem associated with inconsistence and incorrectness of data processing.

Hence, the above discussion on the techniques of prior art have at least two drawbacks. First, the decoded and cached data will be discarded when the command "Host Read" switched to the command "Host Write", and also it will cause delays since the common and single data transmission channel can't be use by the command "Host Write" and the command "Host Read" at one time. Second, while the incessant switch between random two commands occur frequently, it may cause the frequent re-seeking, exhausting the transmission time, and lacking of efficiency, etc.

SUMMARY OF THE INVENTION

A controlling method for data transmission comprising the steps of providing a system bus for connecting a first transmission channel and a second transmission channel with a command processor, adjusting a transmitting direction of the system bus according to a transmitting

direction of the second transmission channel, and proceeding data processing procedures of the second transmission channel according the transmitting direction of the second transmission channel, wherein parts of data processing procedures of the first transmission channel will last during a interval between the system bus adjusting the transmitting direction and the data processing procedures of the second transmission channel start on.

A method for controlling a caching location and a processing timing of data in a data transmission channel module comprising the steps of determining a data transmission channel of the data transmission channel module according to a command issued by a command processor, and parts of processing procedure of a first transmission channel of the data transmission channel module will last for a time interval even though a second transmission channel of the data transmission channel module obtains the ownership of a common transmitting path.

A device apply to an optoelectronic system as a data transmission channel module comprising a first transmission channel bounded by a pair of pipe indices for caching and transmitting data with a first processing procedures; and a second transmission channel bounded by a pair of pipe indices for caching and transmitting data with a second processing procedures.

The present invention providing at least two data transmission channels to ensure that the independence between every data caching and processing reduces the times of flushing the cached data from the data transmission channel and re-seeking through the source, shortening the transmission time, increasing facileness and improving the efficiency of the data transmission.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention will become better understood with regard to the following description, and accompanying drawings where:

Figure 1A is a schematic diagram illustrating the method and device of a buffer as a data transmission channel based on the related art;

Figure 1B is a schematic diagram illustrating the method and device based on an embodiment of the present invention;

Figure 2 is a flowchart of the method for the data transmission channel based on the related art;

Figure 3 is a flowchart illustrating the controlling method and device for data transmission based on an alternative embodiment of the present invention; and

Figure 4 is a timing diagram illustrating the method based on another alternative embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1B a schematic diagram illustrating the method and device of the data transmission channels based on an embodiment of the present invention wherein the device including at least two transmission channel 120 and 130 which constructed for providing an temporary zone needed by the data transmission and buffering, and further coupling to a channel CODEC for data encoding and data decoding (not shown in Figure 1B),

and a bus 140 coupling the first data transmission channel 120 and the second data transmission channel 130 to a command processor (not shown in Figure 1B) such as a host. Furthermore, the first data transmission channel 120 and the second data transmission channel 130 are bounded by a pair of pipe indices 150 including MIDXT 150a and MIDXB 150b and further including a write pipe index WPIDX 151, a decode pipe index DPIDX 152, and a host-pipe sector data send index HPSIDX153 when the corresponding data transmission channel as a decoded data buffer, and a pair of pipe indices 160 including EIDXT 160a and EIDXB 160b and further including a record pipe index RECIDX 161, an encode pipe index ENCIDX 162, and a host-pipe sector data get index HPGIDX 163 when the corresponding data transmission channel as a encoded data buffer, respectively. Since the command is "Host Read", the source data will be cached in the data transmission channel 120, decoded in the channel CODEC, delivered to the bus 140, and then the corresponding pipe indices value will be adjusted. On the other hand, if the command is "Host Write", the source data will be transmitted to and cached in the data transmission channel 130 through the bus 140, encoded, sent to the destination, and then the corresponding pipe indices value will be adjusted.

Figure 3 is a flowchart illustrating the controlling method and device for data transmission based on an alternative embodiment of the present invention. The corresponding data transmission channel and the successive processing procedures including encoding and storing to a peripheral since the command is "Host Write", and decoding the data and delivering the decoded data to the bus 140 since the command is "Host Read" in the step 310. Step 320 is the step for the bus 140 to determine the transmitting

direction based on the second command. In step 330, the data processing procedures of the second command start on, and the parts of data processing procedures of the first data transmission channel keeping on proceeding simultaneously. For example, since the data retrieving process and the data decoding of the first command maybe not proceed in the channel CODEC or use the pickup head (PUH) of the CD-RW drive coincide with the data transmitting to the bus 140 that of the second command, the data processing procedures of the first command may last for a few time. In other words, the concurrence can be achieved since the data processing procedures of two commands may be proceeding in the different elements of the system in a time.

Figure 4 is a timing diagram illustrating the method based on another alternative embodiment of the present invention. Since the first command is "Host Read", label 401 shows that the pickup head and the data transmission channel are both in the decode mode, and the Integrated Device Electronics (IDE) is in the sector data send mode. Once the first command began to be performed and the flag "DISC_WR_Mode" is in the low level, the data retrieved sequentially and cached in the first data transmission channel 120 which resulted in the WPIDX 151 changed values, decoded in the channel CODEC which changed the values of DPIDX 152, and sent to the bus 140 which changed the values of HPSIDX 153. If the successive command is "Host Write", label 402 shows that the bus adjusted the direction to couple to the second data transmission channel 130 and the IDE is in the sector data get mode, and then the data will be cached in the second data transmission channel 130 which resulted in the HPGIDX 163 changed values, and once the flag " DISC_WR_Mode" is in

the high level, the data encoded which changed the values of ENCIDX 162, and then stored in the peripheral which changed the values of RECIDX 161. Besides, label 403 comprises 403a, 403b, and 403c. Once the second command began to be performed, the bus 140 adjusted the transmitting direction and then the values of HPGIDX 153 starts to change whereas the values of HPSIDX 163 stopped to change, as shown in 403a. To the peripheral and the channel CODEC, the conflict will not result from adjusting of the direction of the bus 140, the data retrieving and decoding of the first command could last until the flag "DISC_WR_Mode" pulled to high, as shown in 403b and 403c. Consequently, label 403 shows the characteristic of the present invention.

On the other hand, consider the situation that the first command is "Host Write" and the second one is "Host Read", since the first command began to be performed, the pickup head and the data transmission channel are both in the encode mode, and the IDE is in the sector data get mode. Once the flag "DISC_WR_Mode" is in the high level, the data will be retrieved sequentially from the bus 140 and cached in the second data transmission channel 130 which changed the values of HPGIDX 163, and then encoded in the channel CODEC which changed the values of ENCIDX 162, and sent to the peripheral to store which changed the values of RECIDX 161, as shown in label 404. When the second command began to be performed, the pickup head and the data transmission channel are both in the decode mode, the IDE is in the sector data send mode, the data cached in the first data transmission channel 120, decoded, and sent to the bus 140 whereas changed the values of the WPIDX 151, DPIDX 152, and HPSIDX 153, as shown in the label 405. Besides, label 406 comprises 406a,

406b, and 406c. Since the second command began to be performed, the transmitting direction of the bus 140 will be adjusted, and the values of HPSIDX 153 starts to change whereas the values of HPGIDX 163 stopped to change, as shown in 406a. To the peripheral and the second data transmission channel 130, the conflict will not resulted from the bus 140 adjusting the direction, hence the data encoding and storing will last before the "DISC_WR_Mode" pulled to low level, as shown in 406b and 406c.

In addition, if the successive commands are both "Host Read", and the corresponding data transmission channel has the decoded data which waiting to be processed, then it can be sent to the bus 140 during the interval before the bus 140 changing the transmitting direction, and reduced the times of the "Flush", and hence shortening the transmission time, increasing facileness and improving the efficiency of the data transmission.

Furthermore, suppose that three commands are "Host Read", "Host Write", and "Host Read" respectively, or the sequence is "Host Write", "Host Read", and "Host Write", since the data buffering via corresponding transmission channel, the cached data in the transmission channel should not to be discarded frequently for an accommodation to the successive commands. In other words, since the data transmitting process may utilize the different transmission channel so that the successive processes of the data cached in the data transmission channel will not be interfered with the time that the other command began to be performed and then should be terminated.

While the invention has been described by way of example and in terms of preferred embodiment, it is to be understood that the invention need not be limited to the disclosed embodiments. On the contrary, it is intended to

cover various modifications and similar arrangements included within the spirit of appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.